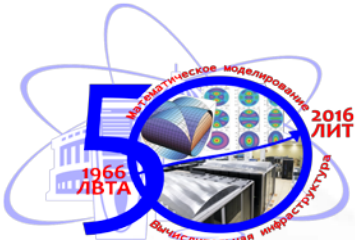




ЛАБОРАТОРИЯ ИНФОРМАЦИОННЫХ ТЕХНОЛОГИЙ

СЕМИНАР ПО ГЕТЕРОГЕННЫМ ВЫЧИСЛЕНИЯМ



Пятница, 24 июня 2016 г. в 15.00

ком. 310

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LDPC codes – design and accelerating simulations

Since Shannon's work from 1948, the topic of error detection and error correction codes, related to channel coding, has seen significant growth. The first serious discussion of error correction codes emerged in Hamming's work in 1950. Today, Low Density Parity Check (LDPC) codes have become very popular because of their general definition and excellent error correcting performance. The design of error correcting codes is a computationally intensive task because of billions operations needed for code evaluation. The presentation will be focused on the optimization of LDPC codes by genetic algorithms and on the discussion of the acceleration of the Belief Propagation (BP) decoder with the use of GPUs. Accelerated simulations based on OpenCL and CUDA were performed on HybriLIT infrastructure. The speed up ratio as compared to CPU simulations will be presented.

