Development of **P**rojectile **S**pectator **D**etector

A.Ivashkin

INR , Moscow

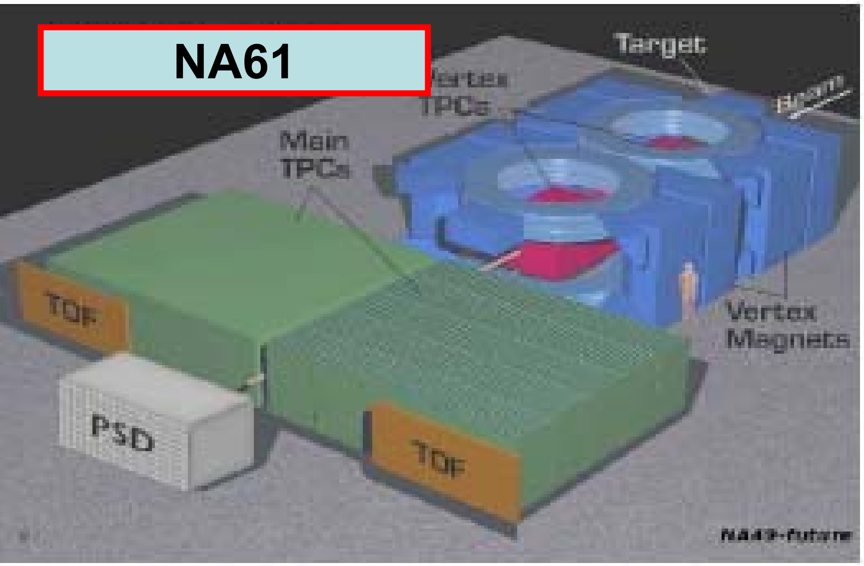
I. **Introduction to PSD.**

II. **Conception and design:**
sampling,
light readout,
signal readout.

III. **Results of beam test of first supermodule.**

IV. **Summary and future plans.**

PSD in NA61 setup.



PSD:

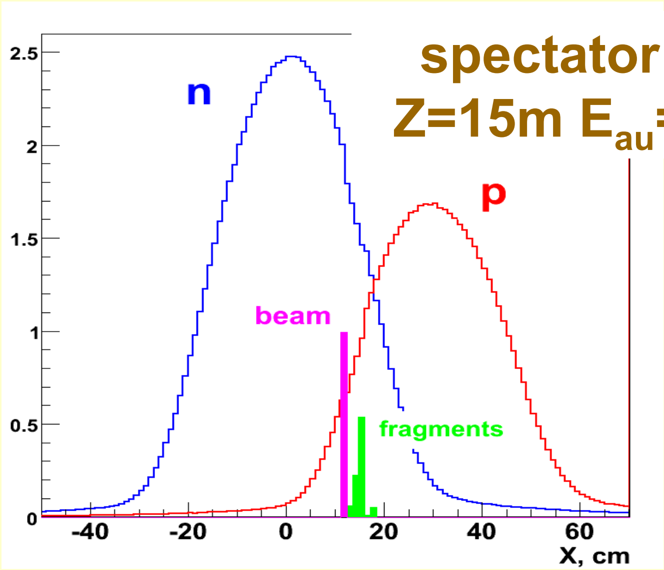
The purpose –
detection of projectile spectators
(non interacting nucleons from projectile ion)

Main Task:
Measurement of event-by-event fluctuations to exclude the fluctuation of participants (geometry of collision)

PSD requirements for NA61:

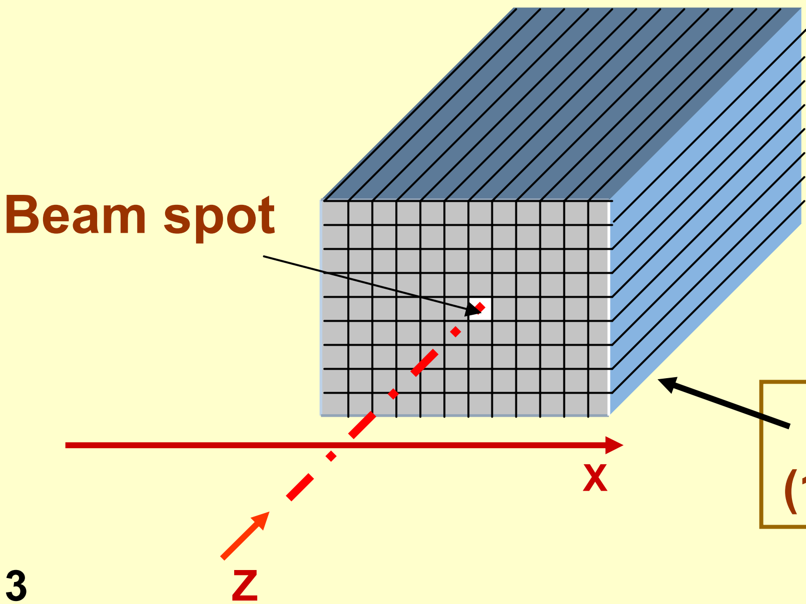
- **Linear response for spectators energy in the range 10 - 30000 GeV.**
- **Challenging energy resolution (~ 50%/sqrt(E)).**
- **Good transverse uniformity of resolution.**
- **Reasonable cost for large volume (~1x1.2 x 1.2 m^3) calorimeter.**

Schematic view of PSD configuration.



spectator spots at
Z=15m E_{au}=15 AGeV

Z	Xcal, (cm)	Ycal, (cm)
10 GeV (z=20m)	200	160
25 GeV (z=20m)	120	90
160 GeV(z=20m)	70	50
10 GeV (Z=15m)	110	100



108 modules
(10x10x120 cm^3 each).

Conception of PSD:

I. Compensation:

$\varepsilon_e / \varepsilon_h = 1$ -- compensated calorimeter.

$\sigma(E)/E = a/\sqrt{E} + b \cdot |1 - \varepsilon_e / \varepsilon_h|$ -- constant term equals to zero.

II. Lead/Scintillator sandwich:

Compensation at Pb:Scint=4:1. For thickness δ_{Pb}=16 mm and δ_{Scint}=4 mm **$\sigma_E/E \sim 50\%/\sqrt{E}$**.

III. Light readout

– WLS-fibers to avoid the Cherenkov radiation.

IV. Signal readout

– Micropixel APD (MAPD) to avoid nuclear counter effect, detection of a few photons signal, compactness, low cost, new technology.

V. Longitudinal segmentation

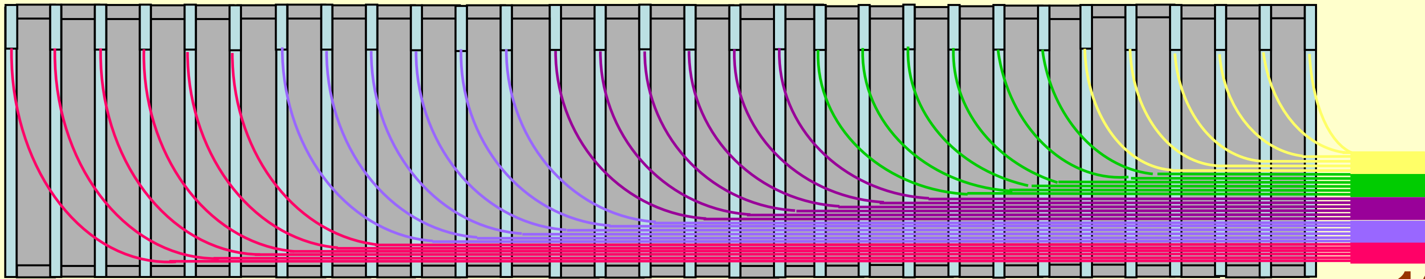
– for permanent calibration of scintillators in radiation hard conditions, uniformity of light collection from WLS-fibers, rejection of electrons.

VI. Modular design

– transverse uniformity of resolution, flexible geometry, simplicity.

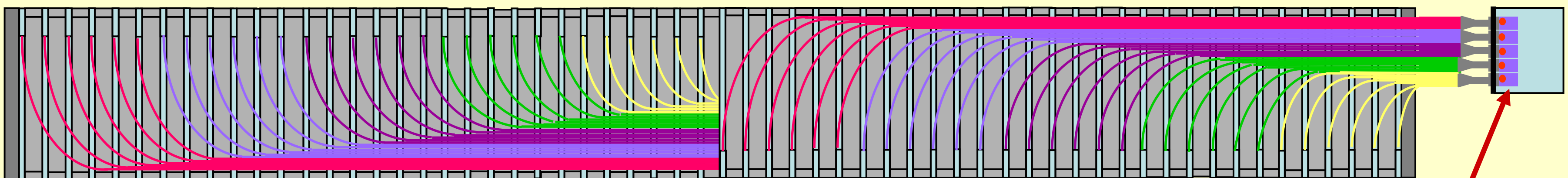
Light readout from scintillators.

Half of module.

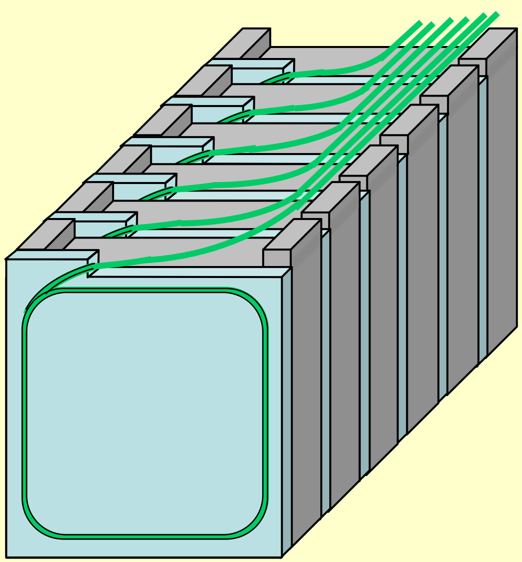


6 fiber/MAPD

10 MAPDs/module

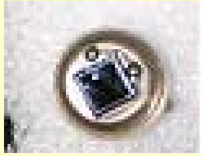


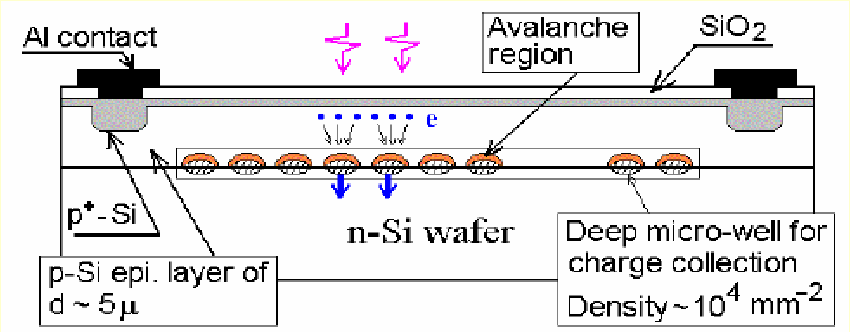
10 Amplifiers
(Gain~40)



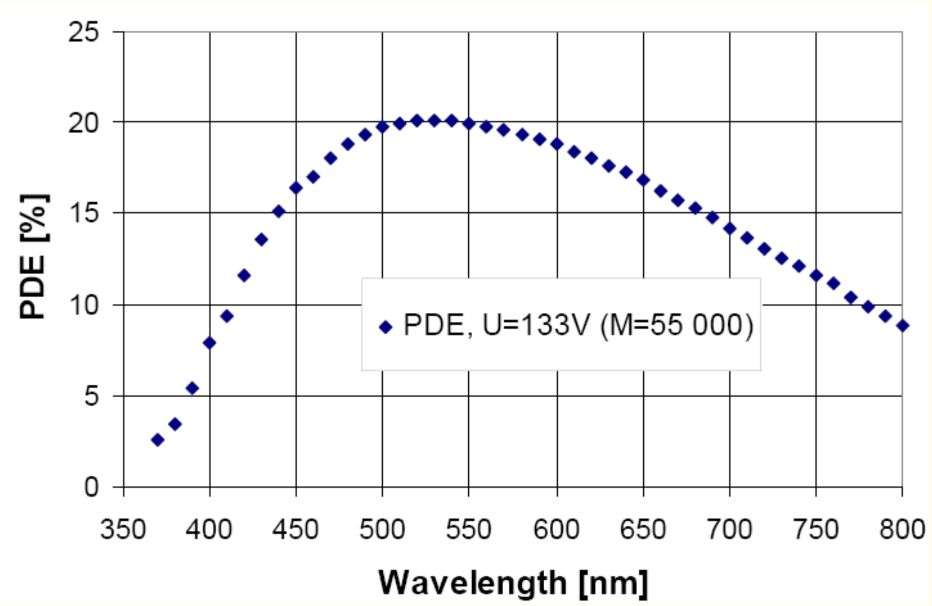
60 lead/scintillator
sandwiches.

Properties of selected MAPDs.





AMPD with deep micro-wells



Type: MW-3d.

Size: 3x3 mm^2.

Number of pixels: $10^4/mm^2$.

Photon detection efficiency:~20%.

Gain: 5-6 $x10^4$.

Working voltage: 130-140V.

Production: Dubna-Mikron.

(Z.Sadygov).

New MAPDs from zecotek.com Co. are available.

Dynamical range of MAPD.

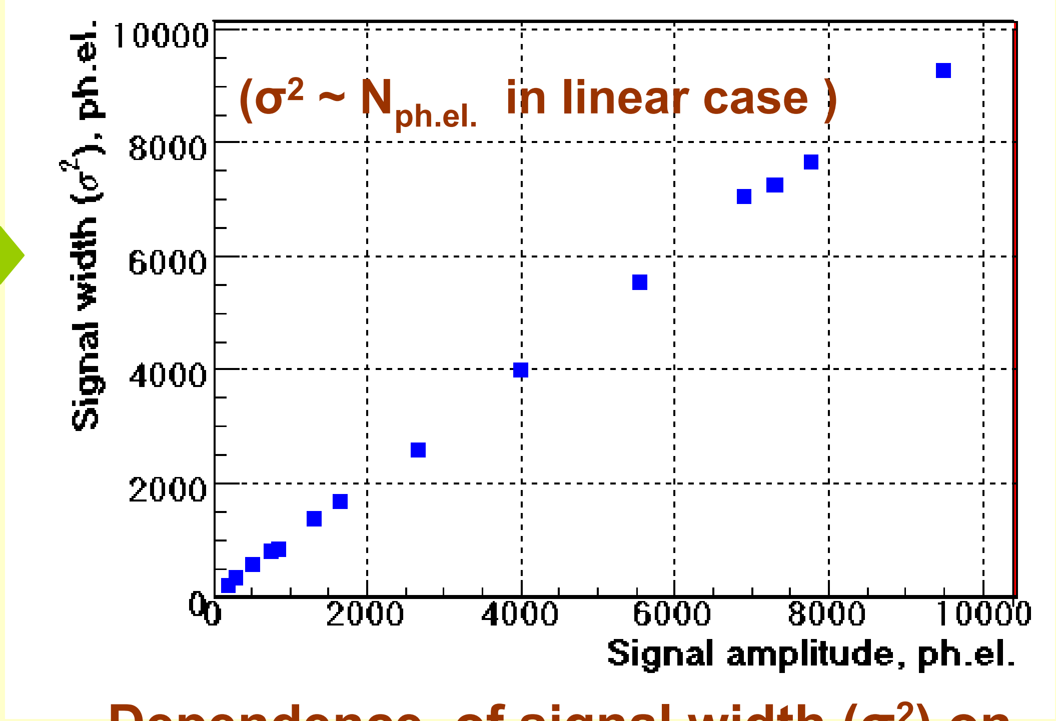
Linearity of response depends on total number of pixels (analytical formula)

$$N_{fired} = N_{total}\left(1 - e^{\frac{-N_{photons}\cdot PDE}{N_{total}}}\right)$$

pixels

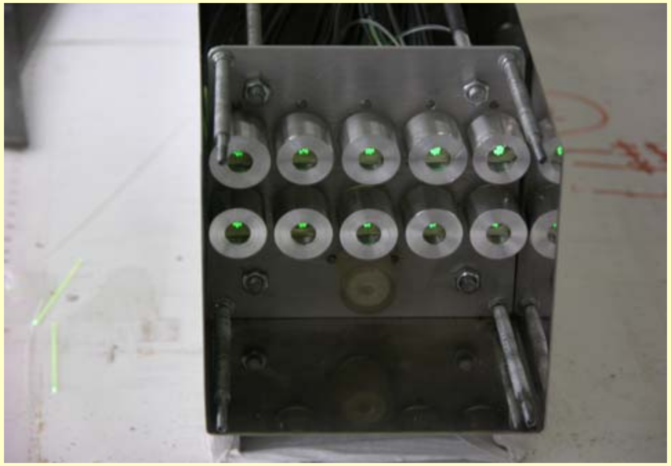
3x3 mm^2 MAPD with pixel density >10^4/mm^2 has a linear response.

Very fine for calorimetry !



Dependence of signal width (σ^2) on signal amplitude $N_{ph.el.}$ in photoelectrons.

Module assembling at INR.



PSD supermodule beam test at NA61

(Sept. 27 – October 1, 2007)

Program of measurements:

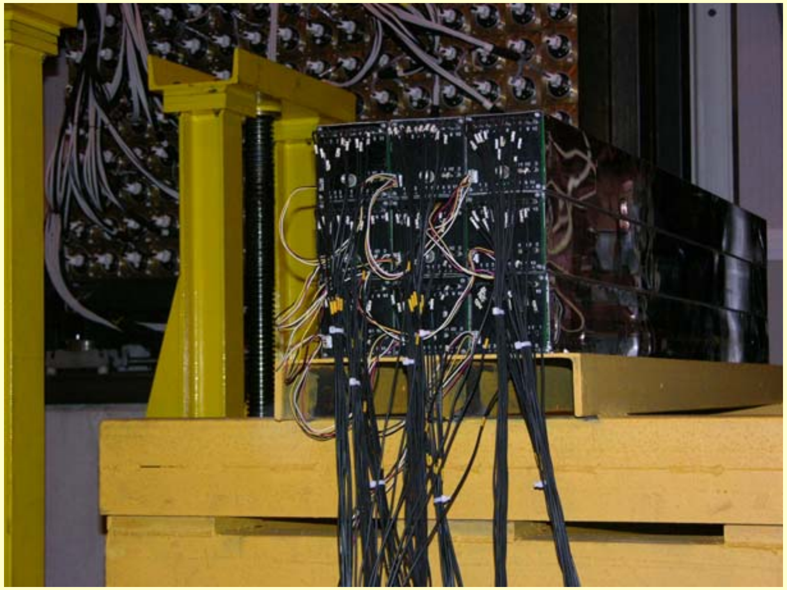
-modules calibration with muon beam;

-study of the response and energy resolution

of the PSD on hadron beams 20, 30, 40, 80, 158 GeV/c;

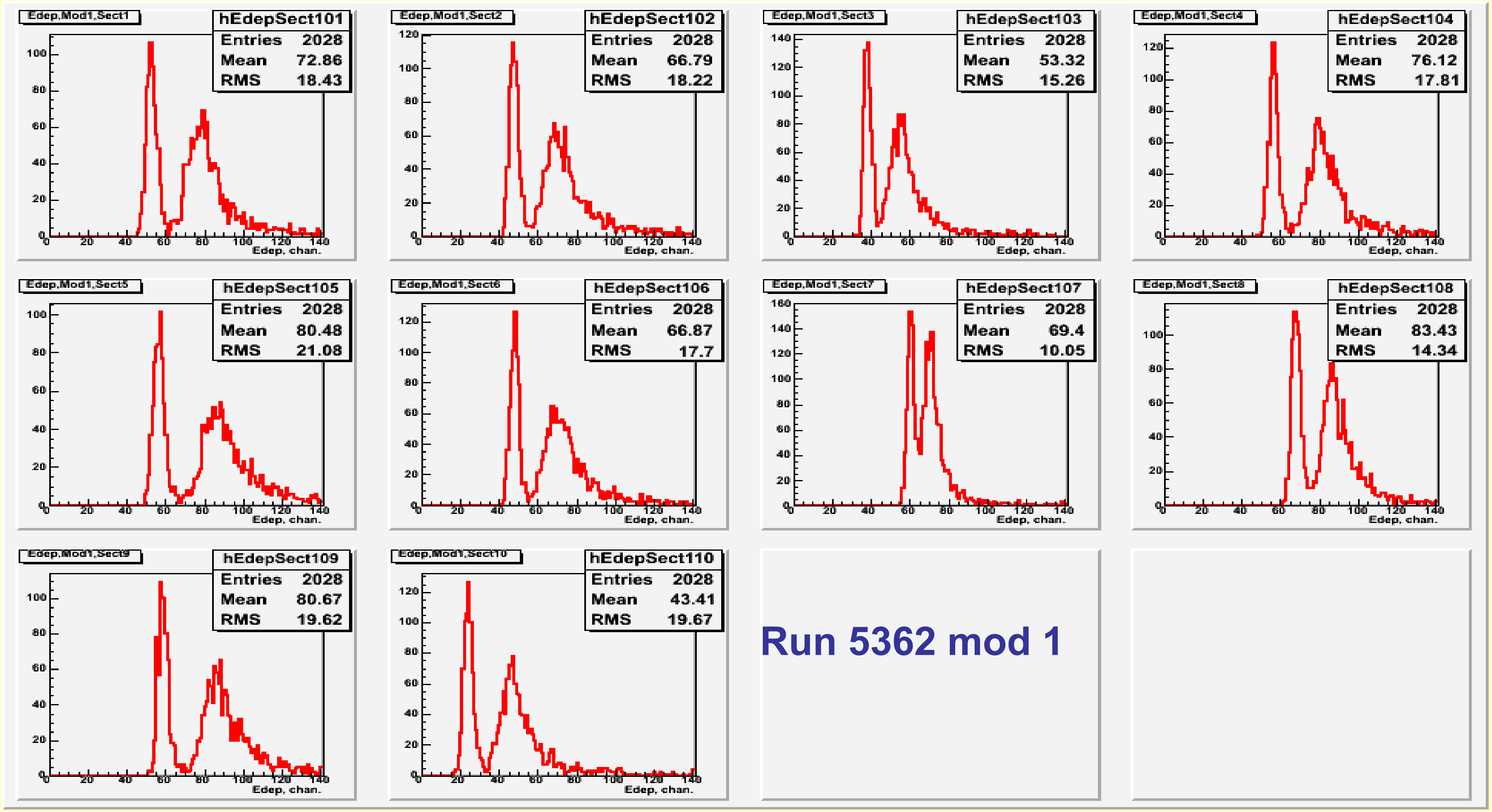
-study of the PSD compesation;

-study of APDs long term stability

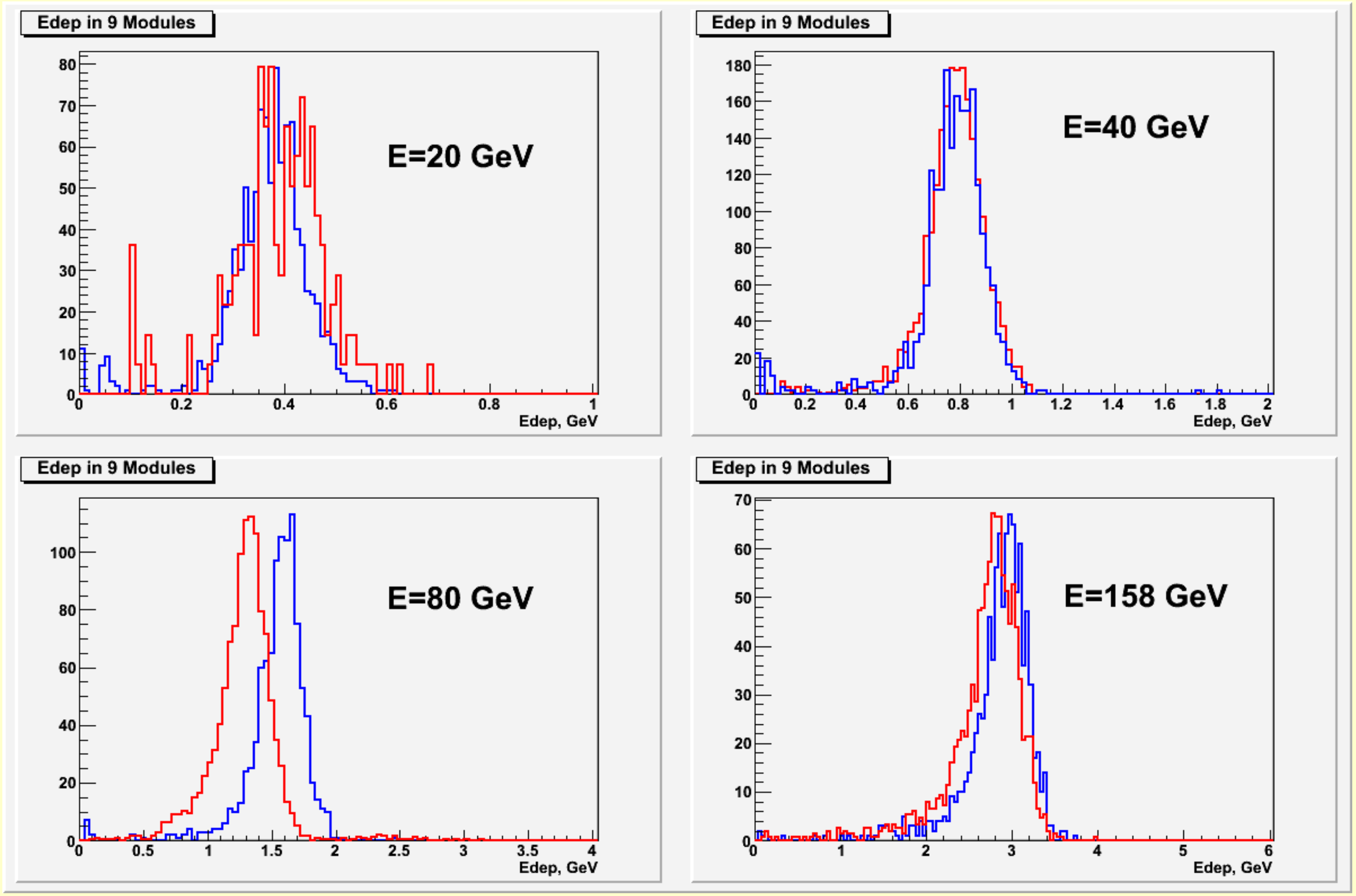


Calibration of modules by muon beam (75 GeV)

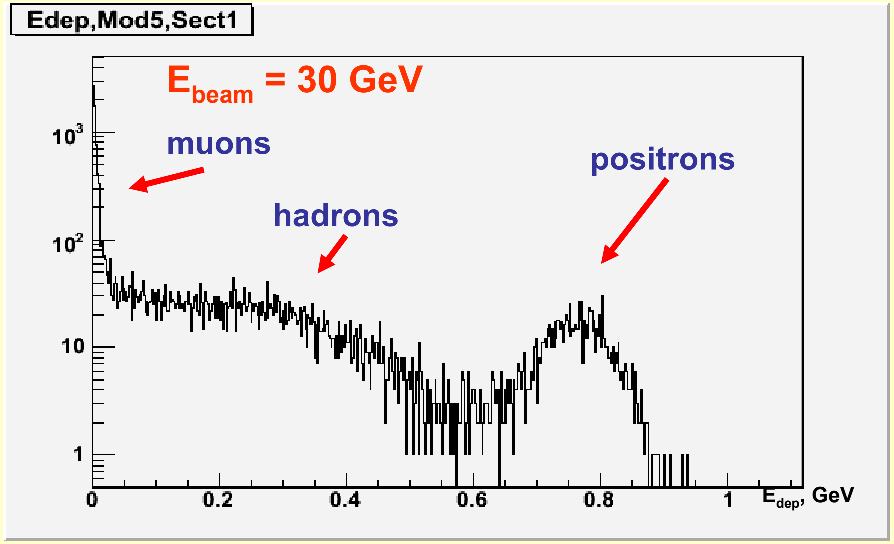
response of first module: experiment



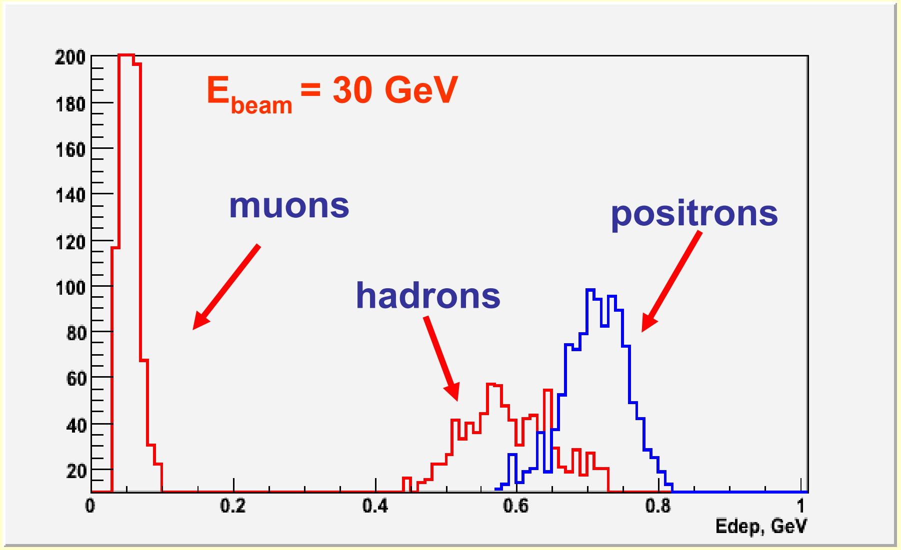
Deposited energy in 9 modules: simulation and experiment



Study of e/h ratio



Energy deposition in 1 section



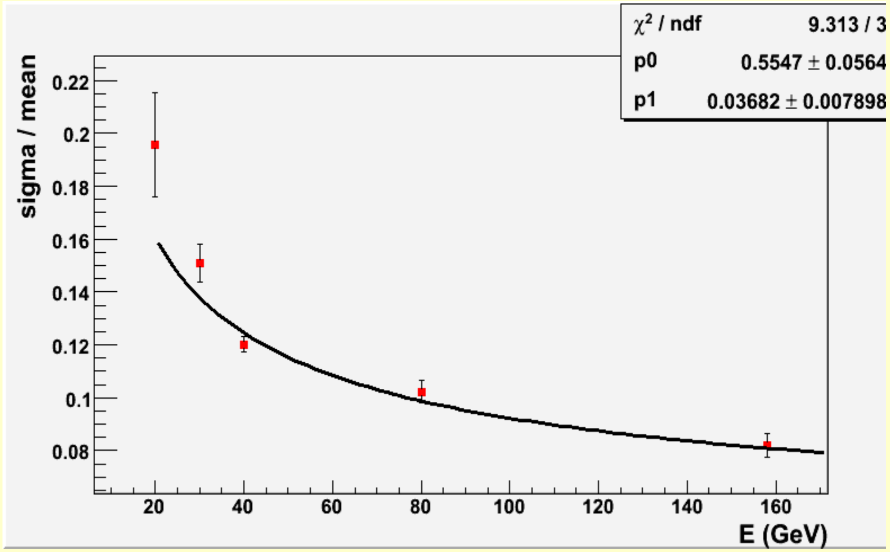
Energy deposition in full supermodule

Energy	EXP	SIM
20	1.36	1.13
30	1.22	-
40	1.16	1.09
60		1.10
80		1.10
150		1.11

e/h ratio

Energy resolution for positrons at E=30GeV is 6.5%

Energy resolution for 9 (3 x 3 area) modules (5 experimental points)

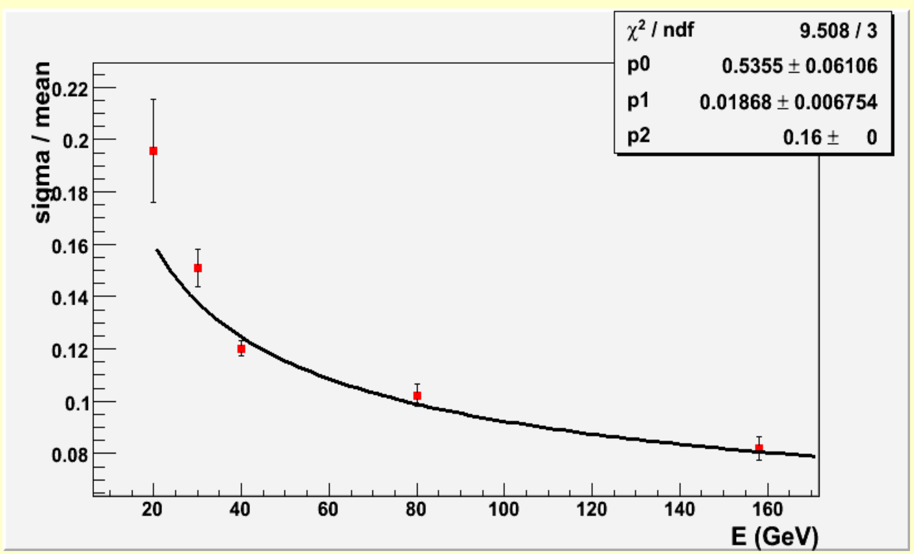


$\sigma(E)/(E)$ = 55.5%/$\sqrt{E(GeV)}$ +3.7%

We introduced shower leakage term according to

NIM A308(1991)481-508

NIM A337(1994)326-341

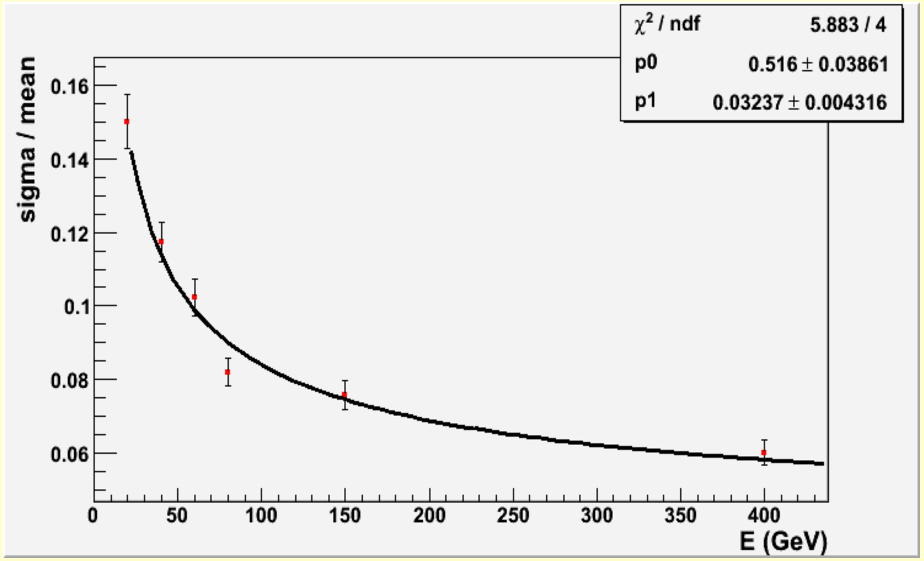


$\sigma(E)/(E)$ = 53.5%/$\sqrt{E(GeV)}$ +1.8%

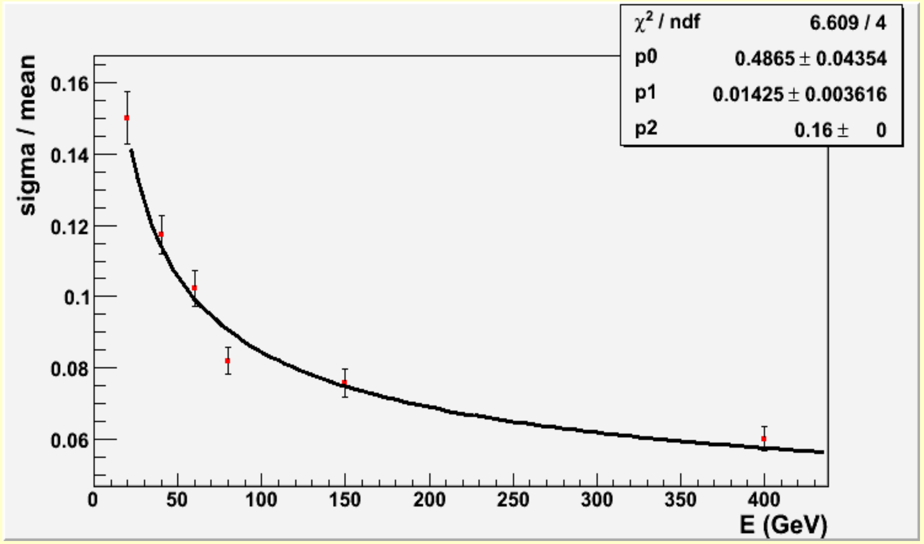
+16%/ $\sqrt[4]{E(GeV)}$

Shower leak 16% -from MC

Energy resolution for 9 (3 x 3 area) modules (MC simulation GEANT3+Geisha)



σ(E)/(E) = 51.6%/√E(GeV) **+3.2%**

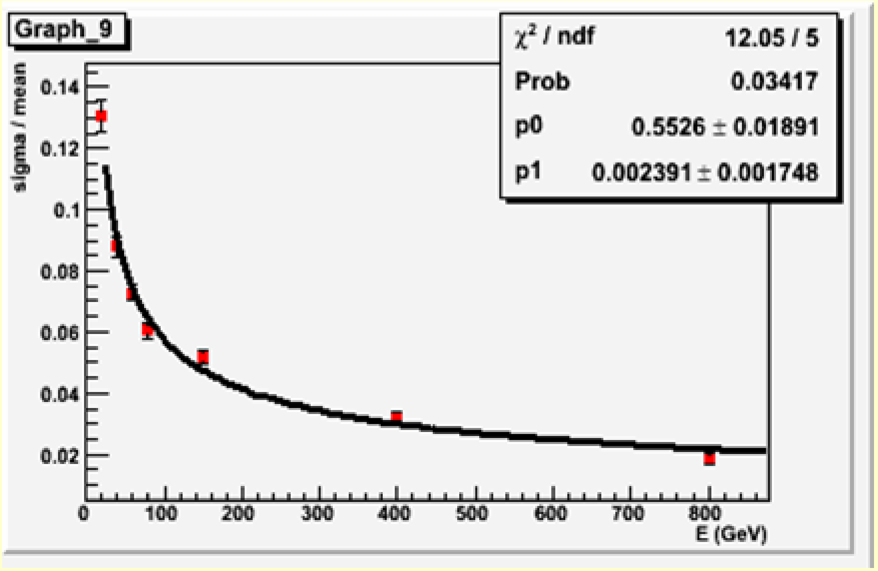


σ(E)/(E) = 48.7%/√E(GeV) **+1.4%**

+16%/ ^{4}√E(GeV)

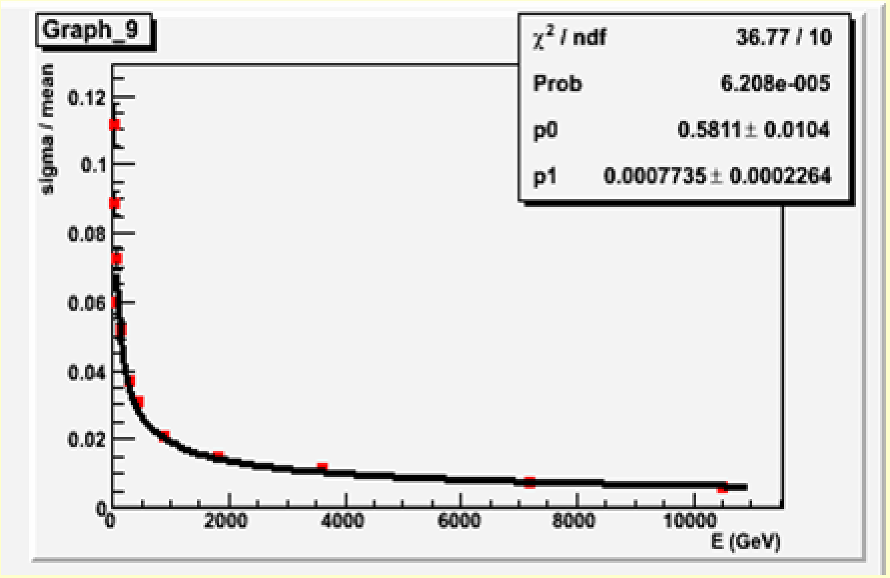
Shower leak

Energy resolution for 9 (3 x 3 area) modules (MC simulation GEANT3+Fluka)



σ(E)/(E) = 55.3%/√E(GeV) +2.3%

(energy range 20-800 GeV)



σ(E)/(E) = 58.1%/√E(GeV) +0.1%

(energy range 20-12000 GeV)

The point above 150 GeV are taken as a sum of a few events with fixed energy of 150 GeV

Some comments on MC results

- MC results depend on the transport code in GEANT.
- Fluka provides more realistic situation (according to LHCb data)
- The constant term in energy resolution becomes negligible in case of event sum this the fixed energy (the case of spectator measurements).
- It might be explained by the fact that the resolution for N spectators depends as sqrt(N):

$$\sigma(E)_N = \sqrt{\Sigma_i \sigma(E)_i^2} = \sqrt{N}\sigma(E)_i$$

i.e. constant term must disappear in spectator measurements (with some approximation).

Summary on PSD performance.

- The experimental energy resolution of PSD 3x3 supermodule is about 55% (stochastic term) plus 3.7% (constant term).
- Correction for the shower leakage improves the resolution as 53% (stochastic term) and 1.8% (constant term).
- According to the current understanding this constant term is essential only for single particle resolution.
- **Simultaneous measurement of N particles with the same energy (NA61 case) leads to the resolution parameterization as:**
  $\sigma(E)_N / E_N = \sigma_1 / E_1 \times 1/\mathrm{sqrt}(N)$,
  where σ_1 and E_1 are resolution and energy for one particle.

Future plans.

- Assembling of 10 or more new PSD modules to arrange 5x5 array of hypermodule.
- Selection of long-term stable MAPDS.
- Development of new front-end electronics.
- Development of PSD DAQ.
- Test of hypermodule at beam.
- Study of energy resolution and transverse unifirmity.

Front-end electronics for PSD

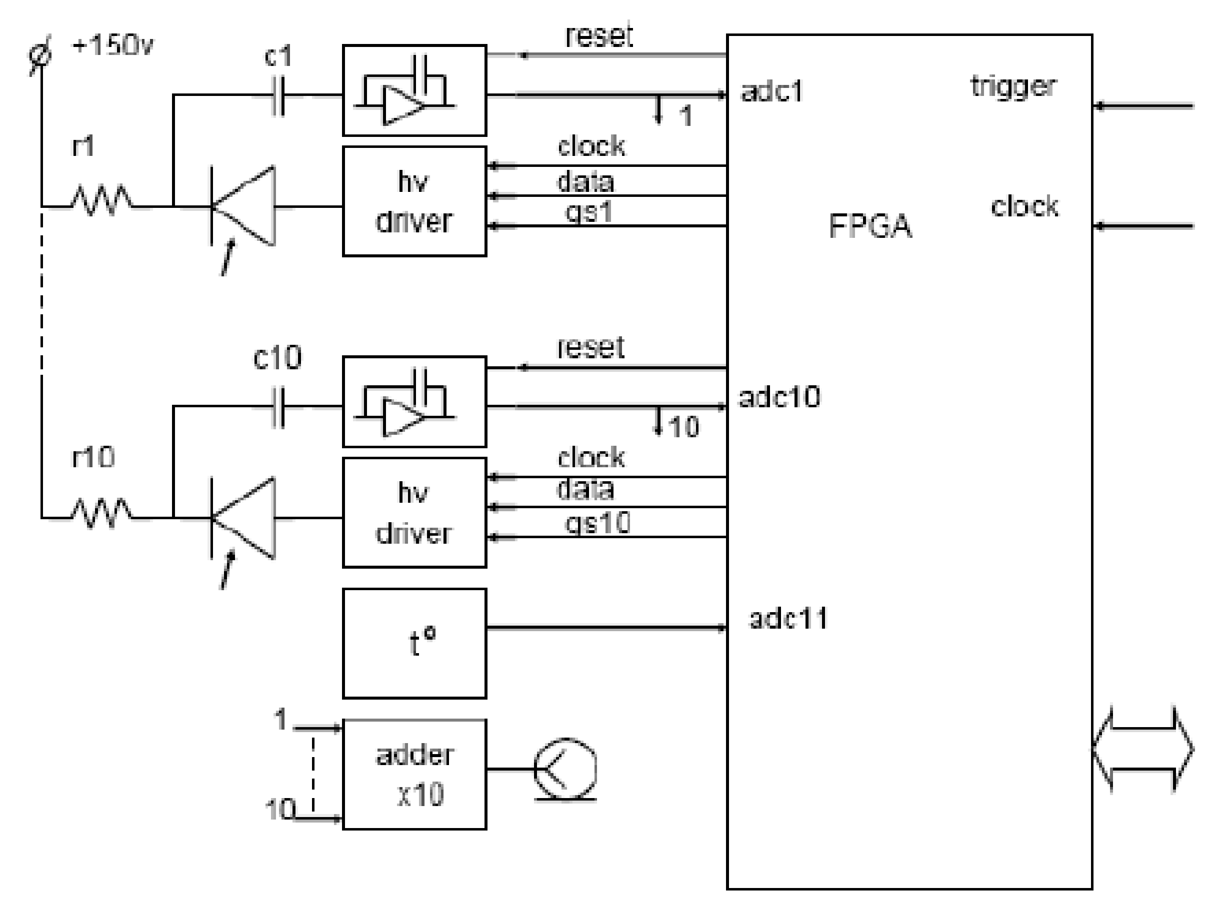


Fig.34 PSD front-end electronics, FEE.

Main elements:

HV driver;

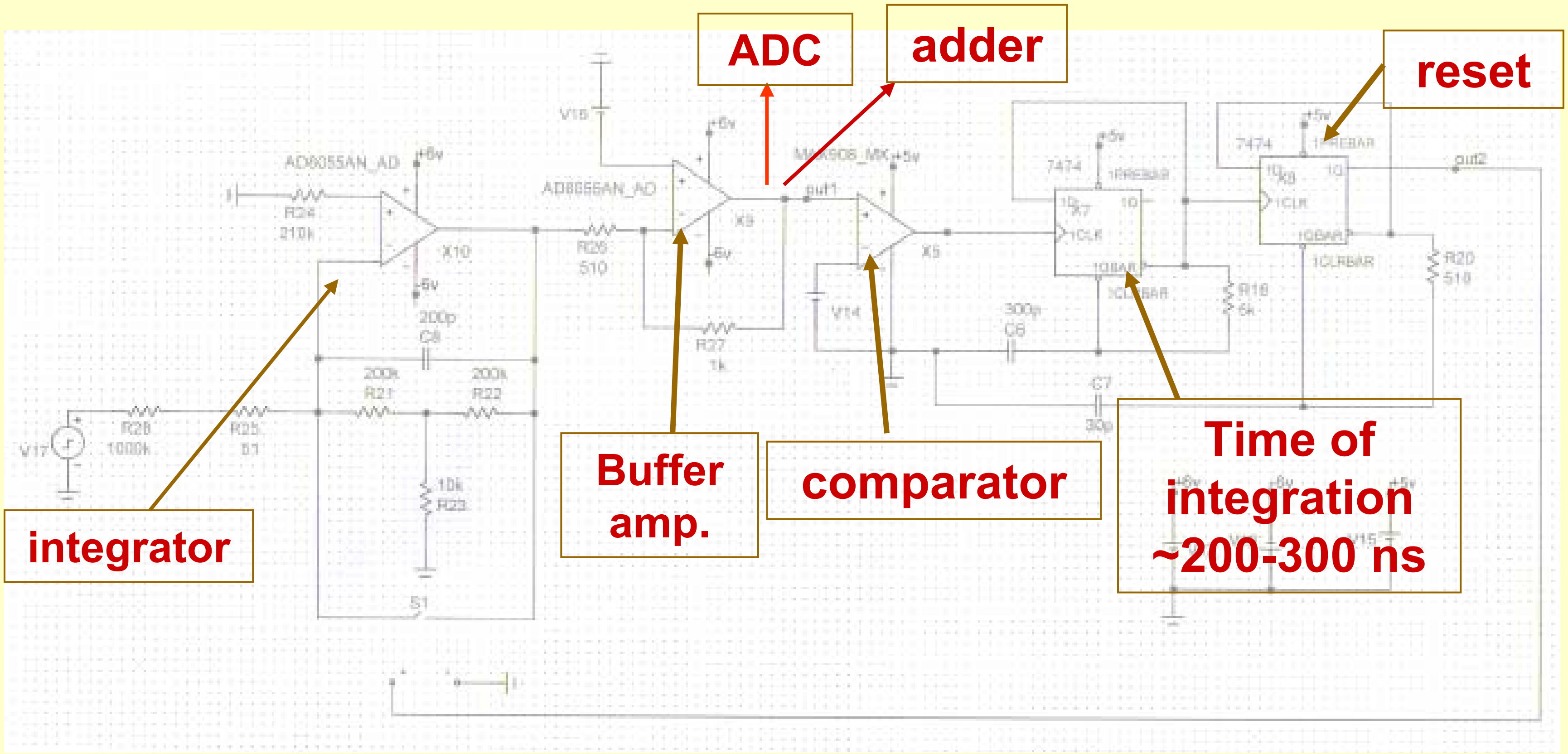
Integrator;

Fast analog adder;

ADC;

FPGA chip.

Conception of PSD module readout



To be established: arrangment of PSD trigger;

Integration to DAQ.

Collaboration is requested!

Variant of PSD DAQ with commercial readout

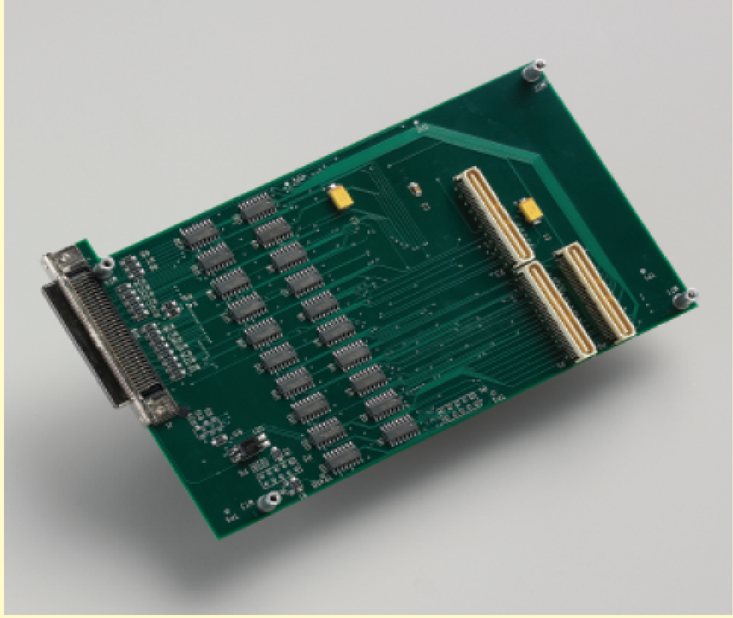
- As a time and cost effective variant of PSD DAQ we suggest to use commercial PMC-PCI cards with 32 (64) LVDS inputs/outputs. The drivers and software are applied. These cards are used in DAQ for large systems.
- This readout must be well matched with proposed integrated FEE.
- There is an opportunity to prepare such DAQ for 2008 beam test.
- Probably, this variant might be accepted for final PSD DAQ if it nicely fits with general NA61 DAQ.
- We have no an experience in operation of such commercial cards. The amount of man power in programming is not known. The collaboration with NA61 participants is urgently requested.

Example of LVDS PCI card

http://www.edt.com/pciss_gs_lvds_rs422.html

edt
a HEICO company

PCI SS/GS LVDS/RS-422



Description

The LVDS/RS-422 mezzanine board provides 33 differential LVDS or RS-422 signals for either the PCI SS or PCI GS main boards. The LVDS/RS-422 signals can be inputs or outputs in groups of four signals. The function of each signal is determined by the FPGA configuration file programmed on the main board.

The PCI SS/GS LVDS/RS-422 mezzanine board is supplied with FPGA configuration files that implement 16 synchronous serial channels. Each channel inputs or outputs a data signal on the edge of the associated clock. The data is stored in or sent from host memory using the PCI DMA. This configuration provides a simple, flexible solution for telemetry, satellite, and monitoring applications.

A large Xilinx Virtex™-E (PCI SS) or Virtex™-II Pro (PCI GS) FPGA and associated memory allow the user to implement an FPGA configuration and process a large amount of serial data. The separate high-speed 16-channel PCI DMA controller allows flexible access to host memory.

Features

- 33 LVDS (standard) or RS-422 (optional) input/output signals
- Transfer rates up to 90 megabits per second using a single channel; 64 megabits per second using all 16 channels
- Provides 16 high-speed DMA channels between LVDS or RS-422 devices and a PCI local bus computer
- User-programmable FPGA up to Xilinx XCV2000E (PCI SS) or XC2VP70 (PCI GS)
- Local memory up to 1 gigabyte (PCI GS)
- Single short PCI local bus slot
- Fast transfers using a 66 MHz 32-bit PCI
- Configuration file for 16 synchronous serial channels

Applications

- Telemetry receiver and transmitter
- Monitoring serial data communications
- Satellite ground station support

Thank you!